IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device analyzer comprising:

a substrate model reading module configured to read, from input data to the semiconductor device analyzer, a substrate network model of three-dimensional meshes representing a substrate of a semiconductor device at a surface of and in which circuit elements are merged;

a Y-matrix entry module configured to prepare a Y-matrix from the substrate network model and express each element of the Y-matrix with a polynomial of differential operator "s";

a discriminating module configured to discriminate internal nodes to be eliminated from and external nodes to be left in the substrate network model; and

a matrix reduction module configured to reduce the Y-matrix by eliminating the internal nodes by repeatedly calculating relationships between four elements of the Y-matrix, associated with internal nodes to be eliminated, without calculating an inverse matrix of the Y-matrix.

Claim 2 (Original): The analyzer of claim 1, further comprising an input unit configured to set an upper limit on the degree of the polynomial of differential operator "s".

Claim 3 (Original): The analyzer of claim 1, further comprising an output format determining module configured to determine an output format for an operation result provided by the matrix reduction module.

Claim 4 (Currently Amended): A method for analyzing a semiconductor device, comprising:

discriminating, among data prescribed in an input format for a circuit simulator, data expressing a substrate network model of three-dimensional meshes representing a substrate of the semiconductor device at a surface of and in which circuit elements are merged;

reading the data expressing the substrate network model;

preparing a Y-matrix from the data expressing the substrate network model;

expressing each element of the Y-matrix with a polynomial of differential operator "s";

discriminating elements of the Y-matrix corresponding to internal nodes to be eliminated from and external nodes to be left in the substrate network model; and

reducing the Y-matrix by eliminating the internal nodes by repeatedly calculating relationships between four elements of the Y-matrix, associated with internal nodes to be eliminated, without calculating an inverse matrix of the Y-matrix.

Claim 5 (Original): The method of claim 4, further comprising externally setting an upper limit on the degree of the polynomial of differential operator "s".

Claim 6 (Original): The method of claim 4, further comprising determining whether or not the dimension of the reduced Y-matrix is equal to the number of the external nodes and iterating, until the dimension of the reduced Y-matrix becomes equal to the number of the external nodes, a sequence including the reading step, Y-matrix preparing step, polynomial expressing step, discriminating step, and Y-matrix reducing step.

Claim 7 (Original): The method of claim 4, further comprising leaving the reduced Y-matrix whose dimension is equal to the number of the external nodes as it is so as to provide stamps.

Claim 8 (Original): The method of claim 4, further comprising determining an output format for the reduced Y-matrix.

Claim 9 (Original): The method of claim 8, wherein the output format is one of a resistive network reconstituted from the reduced Y-matrix, an RC network reconstituted from the reduced Y-matrix, a circuit matrix based on the reduced Y-matrix and representing a multi-port network, and an RC or RCL network of filter circuits based on the reduced Y-matrix.

Claim 10 (Original): The method of claim 4, further comprising reconstituting data in the input format for the circuit simulator from the reduced Y-matrix.

Claim 11 (Original): The method of claim 4, wherein the substrate network model is made of an RC network.

Claim 12 (Currently Amended): A method for manufacturing a semiconductor device, comprising:

discriminating, among data prescribed in an input format for a circuit simulator, data expressing a substrate network model of three-dimensional meshes representing a substrate of the semiconductor device at a surface of and in which circuit elements are merged;

reading the data expressing the substrate network model;

preparing a Y-matrix from the data expressing the substrate network model;

expressing each element of the Y-matrix with a polynomial of differential operator "s";

discriminating elements of the Y-matrix corresponding to internal nodes to be eliminated from and external nodes to be left in the substrate network model;

reducing the Y-matrix by eliminating the internal nodes <u>by repeatedly calculating relationships between four elements of the Y-matrix, associated with internal nodes to be eliminated, without calculating an inverse matrix of the Y-matrix</u>;

reconstituting data in the input format for the circuit simulator from the reduced Y-matrix; and

carrying out a circuit simulation with the reconstituted data for the circuit simulator, to analyze the influence of parasitic elements in the substrate on wiring capacitance of the semiconductor device.

Claim 13 (Original): The method of claim 12, further comprising:

carrying out a process simulation based on required design specifications, to provide doping profiles in the substrate; and

carrying out a device simulation according to the doping profiles provided by the process simulation and given electric boundary conditions so that the data in the circuit simulator input format is provided as the output data of the device simulation.

Claim 14 (Original): The method of claim 13, wherein the device simulation provides device behavior of the semiconductor device as an input data for the circuit simulation.

Claim 15 (Original): The method of claim 12, further comprising determining whether or not a result of the circuit simulation satisfies required circuit performances.

Claim 16 (Original): The method of claim 15, further comprising designing, if the result of the circuit simulation satisfies the required circuit performances, mask patterns based on the data provided by the process simulation, device simulation, and circuit simulation and fabricating a set of masks.

Claim 17 (Original): The method of claim 16, further comprising carrying out a wafer process with use of the set of masks.

Claim 18 (Currently Amended): A computer program product for controlling a semiconductor device analyzer, the program product comprising:

a storage medium readable by the semiconductor device analyzer; and

a program recorded on the storage medium configured to be executed on the semiconductor device analyzer, the program comprising:

discriminating, among data prescribed in an input format for a circuit simulator, data expressing a substrate network model of three-dimensional meshes representing a substrate of the semiconductor device at a surface of and in which circuit elements are merged;

reading the data expressing the substrate network model;

preparing a Y-matrix from the data expressing the substrate network model;

expressing each element of the Y-matrix with a polynomial of differential operator "s";

discriminating elements of the Y-matrix corresponding to internal nodes to be eliminated from and external nodes to be left in the substrate network model; and

reducing the Y-matrix by eliminating the internal nodes by repeatedly calculating relationships between four elements of the Y-matrix, associated with internal nodes to be eliminated, without calculating an inverse matrix of the Y-matrix.

Claim 19 (Original): The computer program product of claim 18, wherein the program further comprises determining whether or not the dimension of the reduced Y-matrix is equal to the number of the external nodes and iterating, until the dimension of the reduced Y-matrix becomes equal to the number of the external nodes, a sequence including the reading, Y-matrix forming, polynomial expressing, discriminating, and Y-matrix reducing.

Claim 20 (Original): The computer program product of claim 18, wherein the program further comprises leaving the reduced Y-matrix whose dimension is equal to the number of the external nodes as it is so as to provide stamps.

Claim 21 (New): The analyzer of claim 1, wherein the matrix reduction module reduces the Y-matrix by repeatedly computing equation of:

$$Y'_{ij} = Y_{ij} - \frac{Y_{jk}Y_{kj}}{Y_{kk}}$$

where Y'_{ij} is an element of the Y-matrix representing admittance between nodes "i" and "j" after reduction and is obtained from elements of the Y-matrix Y_{ij}, Y_{ik}, Y_{kj}, and Y_{kk} of the original Y-matrix, and "k" is the internal node to be eliminated.

Claim 22 (New): The method of claim 4, wherein the Y-matrix is reduced by repeatedly computing equation of:

$$Y'_{ij} = Y_{ij} - \frac{Y_{jk} Y_{kj}}{Y_{kk}}$$

where Y'_{ij} is an element of the Y-matrix representing admittance between nodes "i" and "j" after reduction and is obtained from elements of the Y-matrix Y_{ij}, Y_{ik}, Y_{kj} and Y_{kk} of the original Y-matrix, and "k" is the internal node to be eliminated.

Claim 23 (New): The method of claim 12, wherein the Y-matrix is reduced by repeatedly computing equation of:

$$Y'_{ij} = Y_{ij} - \frac{Y_{jk} Y_{kj}}{Y_{kk}}$$

where Y'_{ij} is an element of the Y-matrix representing admittance between nodes "i" and "j" after reduction and is obtained from elements of the Y-matrix Y_{ij}, Y_{ik}, Y_{kj}, and Y_{kk} of the original Y-matrix, and "k" is the internal node to be eliminated.

Claim 24 (New): The computer program product of claim 18, wherein the Y-matrix is reduced by repeatedly computing equation of:

$$Y'_{ij} = Y_{ij} - \frac{Y_{jk} Y_{kj}}{Y_{kk}}$$

where Y'_{ij} is an element of the Y-matrix representing admittance between nodes "i" and "j" after reduction and is obtained from elements of the Y-matrix Y_{ij}, Y_{ik}, Y_{kj}, and Y_{kk} of the original Y-matrix, and "k" is the internal node to be eliminated.